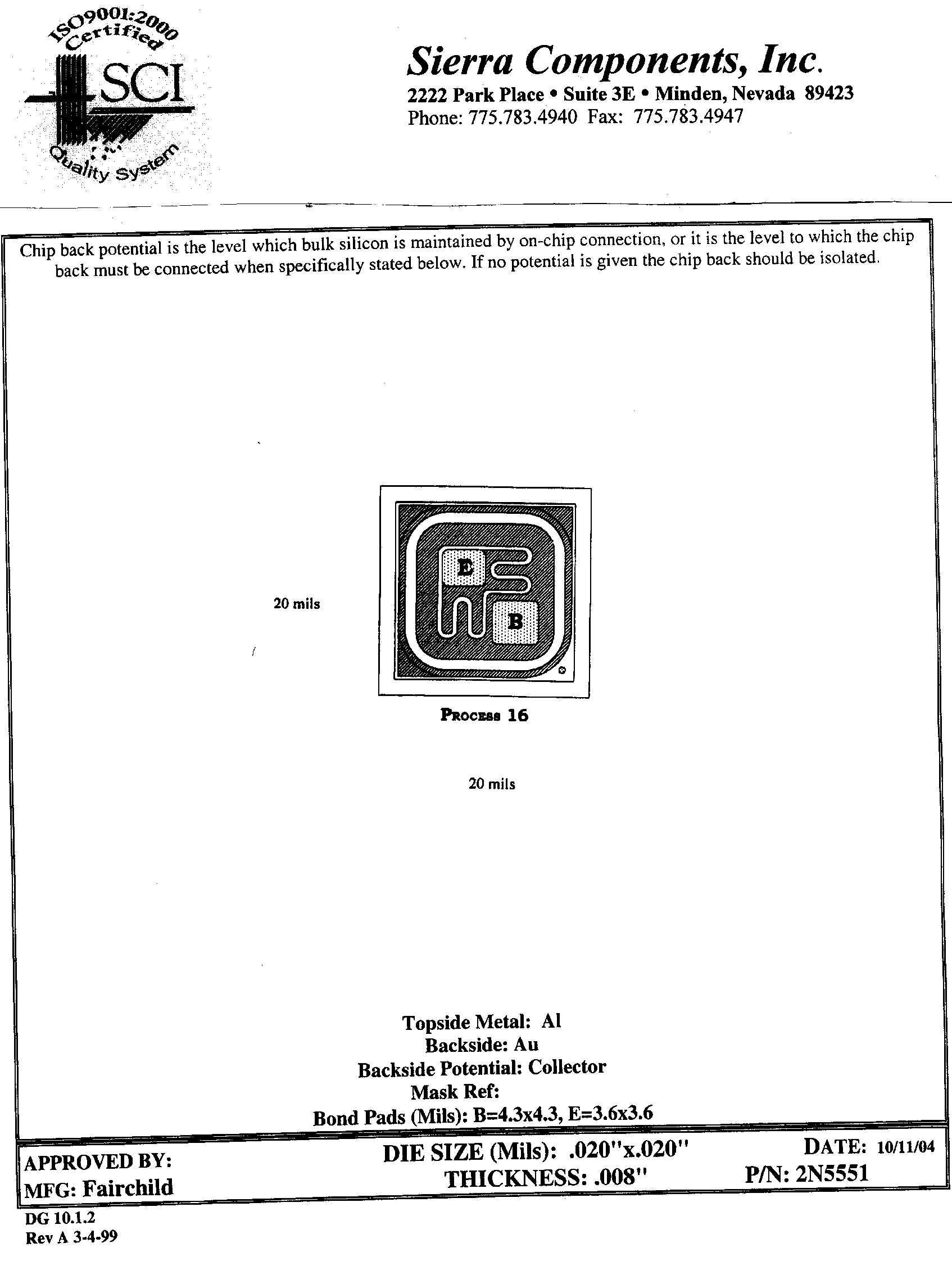
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.020”**

**.020”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0036” X .0036” min.**

**Backside Potential: collector**

**Mask Ref: 16**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 8/7/18**

**MFG: FSC / ON SEMI THICKNESS .008” P/N: 2N5551**

**DG 10.1.2**

#### Rev B, 7/1